Basic Architectural Design of CPT: Analog and Digital Electronics

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Abstract

The architectural design of the analog and digital electronics of the Charged Particle Telescope (CPT) is described. Various design approaches are first discussed. It is recognised that the wide dynamic range required for the LET analog electronics is one of the design drivers. An other obvious requirement is to have a large number of analog channels in CPT.

Two solutions for the analog front-end are discussed. One is based on an integrated preamplifier block with flash A/D conversion. A limited number of discriminators is provided with a very simple trigger conditioning. The data would be collected as pulse heights and as counter data based on the status information from the A/D conversion. The other solution is more conventional. The flash ADC is replaced by a large number of discriminators, which with the associated logic provide trigger conditions, control of the A/D conversion, counter inputs, and comprehensive status information. In this approach the A/D conversion is significantly slower, and a large part of the collected data would be based on counter information.

For digital electronics, two different approaches are considered as well. One is based on the traditional method of routing all the detector signals from the sensors to the electronics box by using cables. All digital functions would be located on one large printed circuit board. The other approach distributes the functions near to the source of the signals. This approach aims to having the analog electronics and the necessary digital functions in the immediate vicinity of the detectors, and transferring only digital signals to the electronics box, where the main data processor would be located. In both cases, the logic would be implemented by using field programmable gate arrays, but for the data processors the requirements would be different.

The selected solution is to use small hybrid boards as the basic building blocks of the sensor electronics. These hybrids will include integrated amplifiers, discriminators, an A/D converter, and logic circuits. One integrated amplifier circuit contains 32 channels. The discriminators are 16 or 32-channel devices, which can be grouped together to obtain the required number of discrimination levels. Rad-hard FPGAs are used as the logic circuits. Both sensors have their own data processor. These are powerful enough to handle all the data analysis tasks. In addition, there is a main processor, which compresses the data, handles the sensor monitoring tasks, and serves as the data interface to the spacecraft.